CHIP SCALE PACKAGE AND METHOD OF ASSEMBLING THE SAME

[01] This application claims the benefit of the co-pending U.S. Provisional Application No. 60/526,082 filed on December 2, 2003, and incorporated herein by reference.

BACKGROUND OF THE INVENTION

[02] Field of the Invention

[03] The present invention generally relates to the field of semiconductors. In particular, the present invention relates to an improved method of assembling a true Chip Scale Package (CSP).

[04] Discussion of Related Art

[05] Semiconductors are materials that have characteristics of insulators and conductors. In today's technology, semiconductor materials have become extremely important as the basis for transistors, diodes, and other solid-state devices. Semiconductors are usually made from germanium or silicon, but selenium and copper oxide, as well as other materials are also used. When properly made, semiconductors will conduct electricity in one direction better than they will in the other direction.

[06] Semiconductor devices and integrated circuits (ICs) are made up of components such as transistors, and diodes, and elements such as resistors and capacitors linked together by conductive connections to form one or more functional circuits. Interconnects on an IC chip serve the same function as the wiring in a conventional circuit.

[07] Wire bonding is a method used to attach very fine metal wire to semiconductor components in order to interconnect the components with each other or with package leads. One problem encountered with wire bonds is the parasitic inductance that arises, which is

based on the size and length of the wire carrying electricity to the components. Wire bonds are also fragile and have limited current carrying capacity.

[08] A flip chip is a leadless monolithic structure, containing circuit elements, which is designed to connect electrically and mechanically to a hybrid circuit. Such a connection may be, but is not limited to, a structure such as a plurality of bumps, which are covered with a conductive bonding agent and are formed on the front-side planar face of the flip chip. In one conventional flip chip mounting technique for integrated circuits, an IC chip is placed front face-down on a mounting base layer element (a substrate) and is connected to wire patterns on the base layer element using the bumps as electrical contacts and the conductive bonding agent as an adhesive. Because the flip chip mounting technique can bond a chip to a base layer element over a much shorter distance than wire bonding, an effect of parasitic inductance can be reduced. Also, the thicker bumps are less fragile than wires and can conduct greater amounts of current. Therefore, some flip chips can be mounted onto a circuit base layer element with limited or even no need for wire bonding, and flip-chip mounting is drawing increasing interest as a mounting technique for high-frequency integrated circuits.

[09] Conventional methods of producing flip-chip packages, however, involve singulating an individual IC chip from a wafer and attaching the singulated IC chip to a substrate. Such individual processing of a single IC chip is highly inefficient in that it is both time-consuming and expensive. Another problem associated with the individual mounting of a singulated IC chip onto a substrate is the difficulty of balancing a single IC chip (e.g. IC chip 10) on a single, central row of bumps (e.g. bumps 5), as illustrated in Figure 1. Therefore, the conventional mounting of an individual IC chip, as described above, requires the use of an IC chip having peripheral bumps or having a full matrix array of bumps.

SUMMARY OF THE INVENTION

[10] A method of producing a chip scale package according to an exemplary embodiment of the present invention comprises mounting an array of two or more IC chips on a substrate and dicing the array, attached to the substrate, into individual chip scale packages, each package including only one IC chip.

[11] A method of producing a chip scale package according to another exemplary embodiment of the present invention comprises providing a wafer and dicing the wafer. The wafer comprises a plurality of IC chips and the wafer is diced into a plurality of chip arrays, each array comprising two or more IC chips. After dicing, each array is mounted on a substrate and then each array, attached to the substrate, is diced into individual chip scale packages, such that each package includes only one IC chip. Each array may comprise a 2 x 2, 3 x 3, or 4 x 4 matrix of IC chips.

[12] A method of producing a chip scale package according to yet another exemplary embodiment of the present invention comprises providing a wafer and dicing the wafer. The wafer comprises a plurality of IC chips, each comprising a plurality of bond pads aligned on an upper surface of the IC chip and a plurality of conductive bumps formed on the plurality of bond pads. The wafer is diced into a plurality of chip arrays, each array comprising two or more IC chips. Each array is then dipped in flux material so that flux material adheres to the bumps on the IC chips of the array. Each array is then mounted on a substrate so that the bumps align with corresponding solder pad openings on an upper surface of the substrate, and so that the flux material adheres the bumps to the solder pad openings. Then, the IC chips of each array are reflowed, thereby melting the bumps and establishing a joint between the IC chips and the substrate. The IC chips, the bumps, and the substrate are then cleaned to remove residual flux material. Then, the IC chips are under fill encapsulated by injecting

encapsulation material into a gap between the IC chips and the substrate. Solder balls are formed on the under surface of the substrate, conductively connected to the bumps. The array, attached to the substrate, is diced into individual chip scale packages, each package comprising only one IC chip.

BRIEF DESCRIPTION OF THE DRAWINGS

[13] These and other features, aspects, and advantages of the present invention will become better understood with reference to the following description, amended claims, and accompanying drawings, which should not be read to limit the invention in any way, in which:

[14] Figure 1 is a perspective view of a conventional IC chip having a central row of bumps;

[15] Figure 2 is a perspective view of a conventional wafer;

[16] Figure 3 is a perspective view of a 2 x 2 array of IC chips, each having a central row of bumps, according to an exemplary aspect of the present invention;

[17] Figure 4 is a perspective view of a 2 x 2 array of IC chips, each having two central rows of bumps, according to an exemplary aspect of the present invention;

[18] Figure 5 is a perspective view of a 2 x 2 array of IC chips, each having a matrix of bumps, according to an exemplary aspect of the present invention;

[19] Figure 6 is a perspective view of an IC chip being mounted on a substrate according to an exemplary aspect of the present invention;

[20] Figure 7 is an enlarged perspective of a portion of the substrate of Figure 6;

[21] Figures 8, 9, and 10 are perspective views of steps of producing a chip scale package according to an exemplary aspect of the present invention;

[22] Figure 11 is a cross-section of a chip scale package according to an exemplary aspect of the present invention; and

[23] Figure 12 is another cross-section of a chip-scale package according to an exemplary aspect of the present invention.

[24] Figure 13 is a flow-chart of an exemplary method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[25] The present invention will be explained in further detail with reference to the accompanying drawings.

[26] Figure 2 is a perspective view of a conventional IC a wafer 200. The wafer 200 is provided in step S1 of an exemplary method according to the present invention, as illustrated in Figure 13.. As discussed, a typical IC wafer comprises a repeated pattern of IC chips 101, which can number into the thousands. For simplicity, Figure 2 depicts only a small number the IC chips 101 which comprise the wafer 200.

[27] Each IC chip 101, includes a plurality of bond pads 104 formed on a top surface thereof. The bond pads 104 are applied through conventional printed circuit technology. A bump 105 (see e.g., Figure 3) is formed on each of the bond pads 104 for the necessary standoff required in subsequent processing. As would be understood by one of skill in the art, the bond pads 104 and the bumps 105 may be aligned as a single row, as illustrated in Figure 3. Alternatively, the bond pads 104 and bumps 105 may be aligned in two or more rows, as illustrated in Figure 4. The two or more rows may be aligned at the center of the chip, as illustrated, or may be peripherally aligned at the edges of the chip. Further, the bond pads 104 and bumps 105 may be disposed in a matrix-like format over the whole surface of the chip, as illustrated in Figure 5. The bumps 105 may be attached at a wafer bumping stage using electroplating or the chip may be solder printed and reflowed to form the bumps. The bumps

105 comprise a conductive material based on the requirements of the package. They may comprise a eutectic alloy of lead/tin for standard packages or may be lead-free for green packages, as would be understood by one of skill in the art.

[28] According to the present exemplary embodiment, a conventional IC wafer, such as wafer 200, is diced into separate chip arrays, (Step S2, Figure 13). Each chip array comprises two or more IC chips. Each array may comprise a 2 x 2, 3 x 3, or 4 x 4 array of IC chips. However, the present invention is not limited to these specific arrays. The number of IC chips comprising an individual array is only limited by the requirements of the under fill encapsulation process (further described below), as would be understood by one of skill in the art. For simplicity, Figures 3 through 6 and 8 through 10 depict a 2 x 2 array 100, including IC chips 101A, 101B, 101C, and 101D. The preparation of chip arrays as described above enables multiple chips within an array to be handled as a single unit and processed together, as described below, rather than individually. This means that the processing is more efficient and less costly than processing chips individually.

[29] After a wafer is diced into chip arrays 100, each array, comprising multiple IC chips, is fixedly attached to a substrate 300, as illustrated in Figures 6 and 8. A plurality of chip arrays may be attached to a single substrate. The substrate 300 can have either a ceramic or organic composition, such as an epoxy-glass resin, or may comprise a variety of other materials as would be understood by one of skill in the art. Further, the substrate 300 may comprise a plurality of layers. As described below, the substrate 300 can later be coupled to a circuit board.

[30] In order to attach the array 100 to the substrate 300, the array 100 is first flipped so that the bumps 105, disposed on the upper face of the IC chip can be mounted to the substrate 300 (Step S3, Figure 13).

[31] As shown in Figures 6 and 7, the substrate comprises solder pad openings 305 on an upper surface thereof. The solder pad openings 305 are conductively coupled through conductive vias 311 to a matrix array of input/outputs (I/Os) 310 disposed on the under surface of the substrate 300. When the array 100 is mounted on the substrate 300, the bumps 105 are conductively coupled to the solder pad openings 305. Thus, the substrate 300 acts as an interposer enabling the redistribution of the I/Os.

[32] After the array 100 is flipped, the array 100 is dipped in a flux material such that some amount of the flux adheres to the bumps 105. (Step S4, Figure 13). The flux agent may vary based on the composition of the bumps 105, for example whether standard bumps are used or whether lead-free bumps are used. The flux thickness is carefully adjusted during the process of attaching the array to the substrate 300, so that the required amount of flux adheres to the bumps 105. The flux adheres to the bumps 105 and to the solder pad openings 305 of the substrate thus enabling the array and the bumps to remain aligned with the solder pad openings.

[33] Once the array 100 is mounted on the substrate 300 (Step S5, Figure 13), the IC chips 101A, 101B, 101C, and 101D are reflowed, thus securing a permanent joint between the IC chips and the substrate 300. (Step S6, Figure 13). Following the reflow, the entire arrangement, including the array of IC chips and the substrate are submitted to a flux cleaning, which removes any amount of flux which remained on the arrangement subsequent to the reflow. (Step S7, Figure 13).

[34] After the flux cleaning step, the IC chips 101A, 101B, 101C, and 101D of the array 100 are encapsulated, as shown in Figure 9. (Step S8, Figure 13). The under fill encapsulation process involves forcing an encapsulation material 401 into the gap between the IC chips 101A, 101B, 101C, and 101D and the substrate 300, around the plurality of bumps 105, as

would be understood by one of skill in the art, and as shown in Figures 11 and 12. The back of the IC chip (facing upward in Figure 9) remains free of any encapsulation material. The encapsulation material 401 can be a polymer-based molding compound or any other of many known encapsulation materials.

[35] The under fill encapsulation material 401 strengthens the final package, helping to prevent shock or vibration from causing the electrical connections between the IC chips 101A, 101B, 101C, and 101D and the substrate 300 to sever. The under fill encapsulation also protects the connections from moisture and contamination.

[36] The under fill encapsulation material 401 is dispensed at one or more sides of the gap between the IC chips 101A, 101B, 101C, and 101D and the substrate 300 and flows by capillary action until it fills the gap and surrounds each of the bumps 105. A low-viscosity under fill encapsulation material can be used to flow into the gap quickly enough to allow for high-speed production.

[37] As an alternative to under fill encapsulation materials, and as would be understood by one of skill in the art, a molding compound that is adapted to flow easily can be applied directly around the array 100 in Figure 8. The molding compound can be, but is not limited to, a thermoplastic molding resin, a thermoset material which can be cured either by thermal or chemical activation, or any conventional molding compound.

[38] Once the array 100 and the substrate 300 have been encapsulated, as described above, solder balls 501, as shown in Figures 11 and 12, are formed or mounted on the underside of the substrate over the I/Os 310. (Step S9, Figure 13).

[39] After the solder balls 501 have been formed on the under surface of the substrate, the entire arrangement is subjected to saw singulation, isolating each of the IC chips 101A, 101B, 101C, and 101D, as shown in Figure 10. (Step S10, Figure 13).

[40] An exemplary individual true CSP, resultant from the above-described process, is illustrated in Figures 11 and 12. As shown, the bumps 105 provide a conductive connection between the IC chip 101A and the upper surface of the substrate 300. The encapsulation material 401 protects this connection and provides the CSP structure with needed support. Once the CSP is mounted on a circuit board (not shown), the bumps 105, the I/Os 310, connected through the substrate to the bumps 105 through the conductive vias 311, as discussed above, and the solder balls 501 provide the necessary conductive connection between the IC chip and the circuit board.

[41] Although the above exemplary embodiments and aspects of the present invention have been described, it will be understood by those skilled in the art that the present invention should not be limited to the described exemplary embodiments, but that various changes and modifications can be made within the spirit and scope of the present invention.